IEEE 802.3bj was developed in response to the rapid growth of server, network and internet traffic. The standard meets the need for higher data rates over backplanes and copper cables for 100 Gbit/s throughput.

IEEE 802.3bj RS Decoder

Key benefits of the decoder are:

- High-throughput, low-latency decoder core.
- Support for single channel mode (100 Gbit/s).
- Support for bypass mode with low latency.
- Symbol error measurement per lane.
- Detection of uncorrectable code words.
- Easy-to-use handshaking interfaces.
- Available for ASIC and FPGAs.

IEEE 802.3bj RS Encoder

Key benefits of the encoder are:

- High-throughput, low-latency encoder core.
- Support for single channel mode (100 Gbit/s).
- Easy-to-use interfaces.
- No RAM required.
- Available for ASIC and FPGAs.

Performance Figures

- 100 Gbit/s coded throughput at 625 MHz.
- Decoding latency of 92.8 ns at 625 MHz.
- Latency of 1.6 ns at 625 MHz in bypass mode.
- Bit Error Rate 10^{-11} at 8.8 dB (E_B/N_0).
- Block Error Rate 10^{-8} at 8.7 dB (E_B/N_0).

Features

- Compliant with IEEE 802.3bj, Clause 91
- Support for (528, 514) Reed-Solomon (RS) code
- Corrects up to seven erroneous symbols

Applications

- 100 Gigabit Ethernet over backplane
- Applications with highest throughput requirements

Deliverables

- VHDL or Verilog source code or synthesized netlist
- HDL simulation models e.g. for Aldec's Riviera-PRO
- VHDL or SystemC testbench
- bit-accurate Matlab, C or C++ simulation model
- comprehensive documentation

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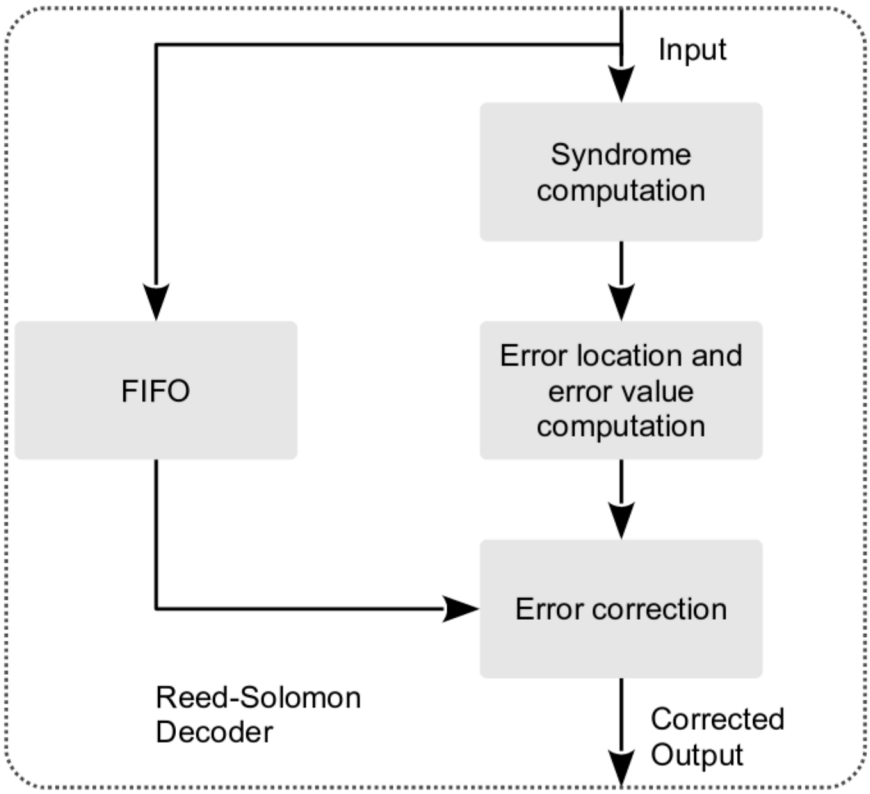
Decoder Block Diagram

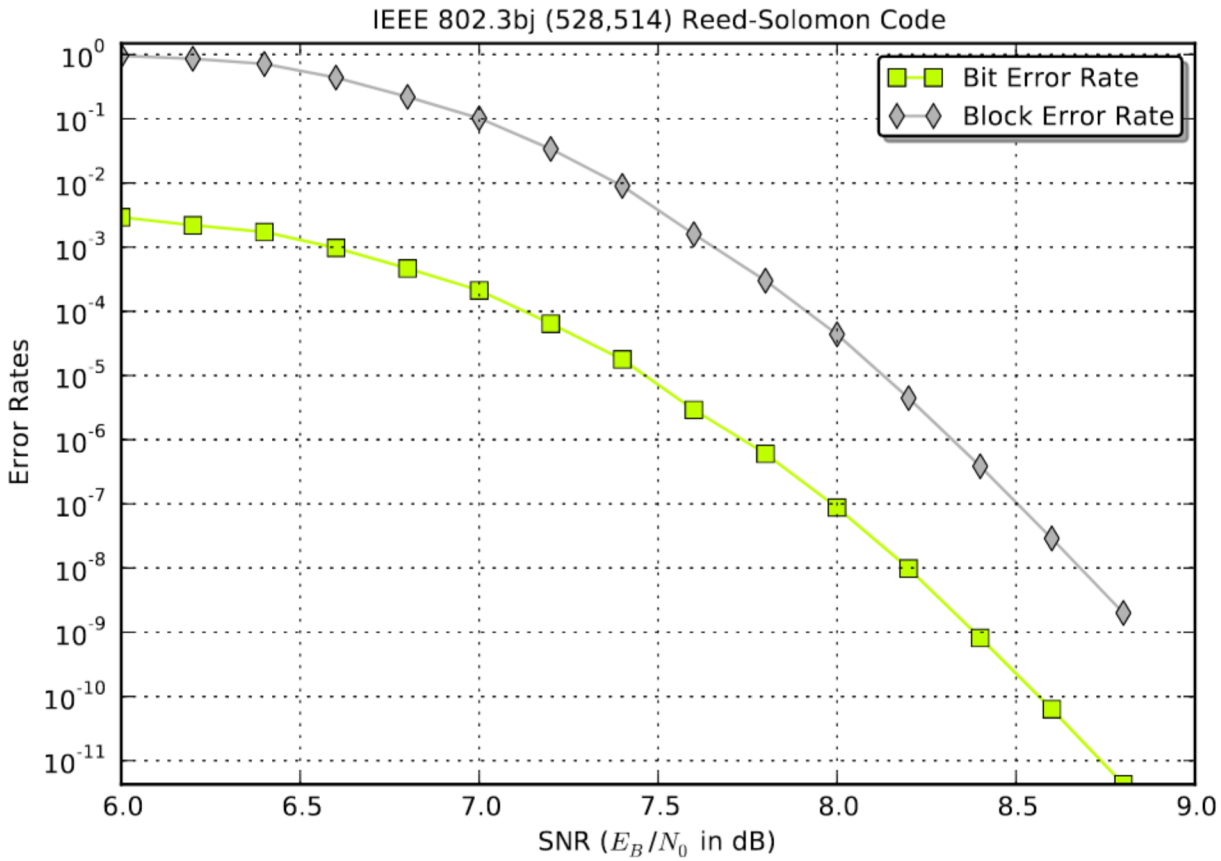
The following figure depicts the architecture of the Reed-Solomon decoder. It consists of

- a syndrome computation unit,
- a unit for computation of the error location and error value polynomials,
- an error correction unit, and
- a FIFO.



Error Correction Performance

The following figure depicts the error correction performance of the (528, 514) Reed-Solomon code.



Related Products

Generic Open Source Viterbi Decoder

WiMedia 1.5 UWB LDPC Decoder

802.11n/ac LDPC Decoder

About Creonic

Creonic is an ISO 9001:2008 certified provider of ready-for-use IP cores for several algorithms of communications such as forward error correction (LDPC and Turbo coding), synchronization, and MIMO. The company offers the richest product portfolio in this field, covering standards like DVB-S2X, LTE-A, DVB-RCS2, DOCSIS 3.1, CCSDS, WiFi, WiGig, and UWB. The products are applicable for ASIC and FPGA technology and comply with the highest requirements with respect to quality and performance. For more information, please visit www.creonic.com.

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